8-BIT MICROCONTROLLER

Table of Contents-

1. GENERAL DESCRIPTION

The W78E516B is an 8-bit microcontroller which has an in-system programmable Flash EPROM for firmware updating. The instruction set of the W78E516B is fully compatible with the standard 8052. The W78E516B contains a 64K bytes of main Flash EPROM and a 4K bytes of auxiliary Flash EPROM which allows the contents of the 64KB main Flash EPROM to be updated by the loader program located at the 4KB auxiliary Flash EPROM ROM; 512 bytes of on-chip RAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 4-bit port P4; three 16-bit timer/counters; a serial port. These peripherals are supported by a eight sources two-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78E516B allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

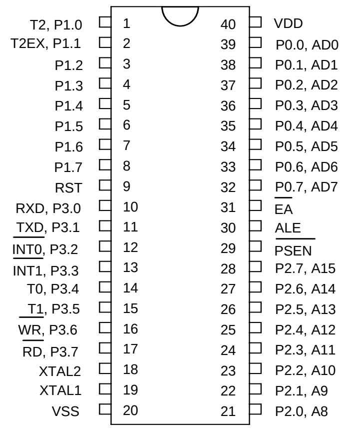
The W78E516B microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

2. FEATURES

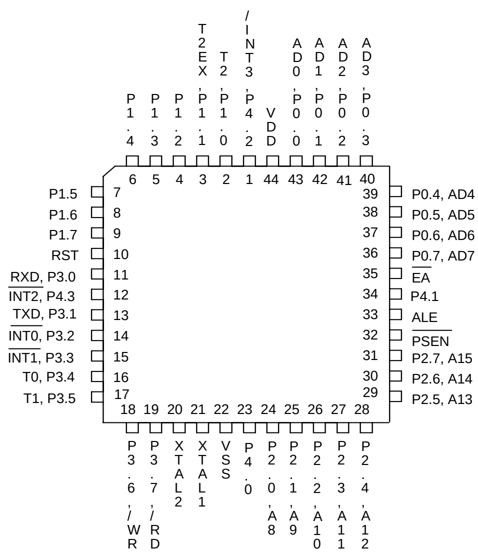
- Fully static design 8-bit CMOS microcontroller up to 40 MHz.
- 64K bytes of in-system programmable Flash EPROM for Application Program (APROM).
- 4K bytes of auxiliary Flash EPROM for Loader Program (LDROM).
- 512 bytes of on-chip RAM. (including 256 bytes of AUX-RAM, software selectable)
- 64K bytes program memory address space and 64K bytes data memory address space.
- Four 8-bit bi-directional ports.
- One 4-bit multipurpose programmable port.
- Three 16-bit timer/counters
- One full duplex serial port
- Six-sources, two-level interrupt capability
- Built-in power management
- Code protection
- Packaged in
  - – Lead Free (ROHS) DIP 40: W78E516B40DL
  - – Lead Free (ROHS) PLCC 44: W78E516B40PL
  - – Lead Free (ROHS) PQFP 44: W78E516B40FL

3. PIN CONFIGURATIONS

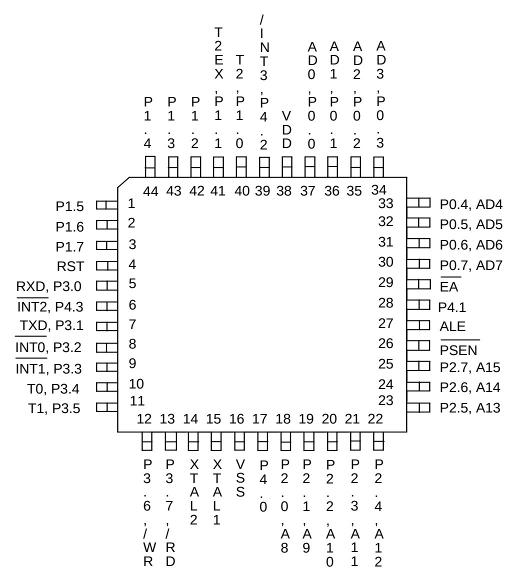
40-Pin DIP



44-Pin PLCC



44-Pin QFP



4. PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTIONS
$\overline{EA}$	I	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute the external ROM. The ROM address and data will not be presented on the bus if the $\overline{EA}$ pin is high.
$\overline{PSEN}$	O H	PROGRAM STORE ENABLE: $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O H	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency.
RST	I L	RESET: A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	I	CRYSTAL 1: This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	O	CRYSTAL 2: This is the crystal oscillator output. It is the inversion of XTAL1.
VSS	I	GROUND: ground potential.
VDD	I	POWER SUPPLY: Supply voltage for operation.
P0.0 – P0.7	I/O D	PORT 0: Function is the same as that of standard 8052.
P1.0 – P1.7	I/O H	PORT 1: Function is the same as that of standard 8052.
P2.0 – P2.7	I/O H	PORT 2: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.
P3.0 – P3.7	I/O H	PORT 3: Function is the same as that of the standard 8052.
P4.0 – P4.3	I/O H	PORT 4: A bi-directional I/O. See details below.

*** Note: TYPE** I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain

PORT4

Another bit-addressable port P4 is also available and only 4 bits (P4<3:0>) can be used. This port address is located at 0D8H with the same function as that of port P1.

Example:

```
P4      REG     0D8H
MOV     P4, #0AH          ; Output data "A" through P4.0 – P4.3.
MOV     A, P4             ; Read P4 status to Accumulator.
ORL     P4, #00000001B
ANL     P4, #11111110B
```

5. FUNCTIONAL DESCRIPTION

The W78E516B architecture consists of a core controller surrounded by various registers, four general purpose I/O ports, one special purpose programmable 4-bits I/O port, 512 bytes of RAM, three timer/counters, a serial port and an internal 74373 latch and 74244 buffer which can be switched to port2. The processor supports 111 different opcodes and references both a 64K program address space and a 64K data storage space.

5.1 RAM

The internal data RAM in the W78E516B is 512 bytes. It is divided into two banks: 256 bytes of scratchpad RAM and 256 bytes of AUX-RAM. These RAMs are addressed by different ways.

- RAM 0H – 7FH can be addressed directly and indirectly as the same as in 8051. Address pointers are R0 and R1 of the selected register bank.
- RAM 80H – FFH can only be addressed indirectly as the same as in 8051. Address pointers are R0, R1 of the selected registers bank.
- AUX-RAM 0H – FFH is addressed indirectly as the same way to access external data memory with the MOVX instruction. Address pointer are R0 and R1 of the selected register bank and DPTR register. An access to external data memory locations higher than FFH will be performed with the MOVX instruction in the same way as in the 8051. The AUX-RAM is disable after a reset. Setting the bit 4 in CHPCON register will enable the access to AUX-RAM. When AUX-RAM is enabled the instructions of "MOVX @Ri" will always access to on-chip AUX-RAM. When executing from internal program memory, an access to AUX-RAM will not affect the Ports P0, P2, $\overline{WR}$ and $\overline{RD}$.

Example,

```
CHPENR   REG      F6H
CHPCON   REG      BFH
MOV      CHPENR, #87H
MOV      CHPENR, #59H
ORL      CHPCON, #00010000B    ; enable AUX-RAM
MOV      CHPENR, #00H
MOV      R0, #12H
MOV      A, #34H
MOVX     @R0, A                ; Write 34h data to 12h address.
```

5.2 Timers 0, 1 and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0, 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2. The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

5.3 Clock

The W78E516B is designed with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used by default. This makes the W78E516B relatively insensitive to duty cycle variations in the clock.

5.4 Crystal Oscillator

The W78E516B incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground, and a resistor must also be connected from XTAL1 to XTAL2 to provide a DC bias when the crystal frequency is above 24 MHz.

5.5 External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator. As a result, the external clock signal should have an input one level of greater than 3.5 volts.

5.6 Power Management

Idle Mode

Setting the IDL bit in the PCON register enters the idle mode. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-down Mode

When the PD bit in the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator. To exit from power-down mode is by a hardware reset or external interrupts $\overline{INT0}$ to $\overline{INT1}$ when enabled and set to level triggered.

5.7 Reduce EMI Emission

The W78E516B allows user to diminish the gain of on-chip oscillator amplifier by using programmer to clear the B7 bit of security register. Once B7 is set to 0, a half of gain will be decreased. Care must be taken if user attempts to diminish the gain of oscillator amplifier, reducing a half of gain may affect the external crystal operating improperly at high frequency above 24 MHz. The value of R and C1, C2 may need some adjustment while running at lower gain.

5.8 Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the W78E516B is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line. During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

W78E516B Special Function Registers (SFRs) and Reset Values

F8									FF
F0	+B 00000000						**CHPENR 00000000**		F7
E8									EF
E0	+ACC 00000000								E7
D8	**+P4 xxxx1111**								DF
D0	+PSW 00000000								D7
C8	+T2CON 00000000		RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			CF
C0	XICON 00000000		**P4CONA 00000000**	**P4CONB 00000000**	**SFRAL 00000000**	**SFRAH 00000000**	**SFRFD 00000000**	**SFRCN 00000000**	C7
B8	+IP 00000000							**CHPCON 0xx00000**	BF
B0	+P3 00000000				**P43AL 00000000**	**P43AH 00000000**			B7
A8	+IE 00000000				**P42AL 00000000**	**P42AH 00000000**	**P2ECON 0000XX00**		AF
A0	+P2 11111111								A7
98	+SCON 00000000	SBUF xxxxxxxx					**P2EAL 00000000**	**P2EAH 00000000**	9F
90	+P1 11111111				**P41AL 00000000**	**P41AH 00000000**			97
88	+TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8F
80	+P0 11111111	SP 00000111	DPL 00000000	DPH 00000000	**P40AL 00000000**	**P40AH 00000000**		PCON 00110000	87

Notes:

1. The SFRs marked with a plus sign(+) are both byte- and bit-addressable.
2. The text of SFR with bold type characters are extension function registers.

5.9 Port 4

Port 4, address D8H, is a 4-bit multipurpose programmable I/O port. Each bit can be configured individually by software. The Port 4 has four different operation modes.

Mode 0: P4.0 – P4.3 is a bi-directional I/O port which is same as port 1. P4.2 and P4.3 also serve as external interrupt $\overline{\text{INT3}}$ and $\overline{\text{INT2}}$ if enabled.

Mode 1: P4.0 – P4.3 are read strobe signals that are synchronized with $\overline{\text{RD}}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

Mode 2: P4.0 – P4.3 are write strobe signals that are synchronized with $\overline{\text{WR}}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

Mode 3: P4.0 – P4.3 are read/write strobe signals that are synchronized with $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

When Port 4 is configured with the feature of chip-select signals, the chip-select signal address range depends on the contents of the SFR P4xAH, P4xAL, P4CONA and P4CONB. The registers P4xAH and P4xAL contain the 16-bit base address of P4.x. The registers P4CONA and P4CONB contain the control bits to configure the Port 4 operation mode.

5.10 $\overline{\text{INT2}}$ / $\overline{\text{INT3}}$

Two additional external interrupts, $\overline{\text{INT2}}$ and $\overline{\text{INT3}}$, whose functions are similar to those of external interrupt 0 and 1 in the standard 80C52. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 80C52. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB ($\overline{\text{CLR}}$) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

XICON - external interrupt control (C0H)

PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

PX3: External interrupt 3 priority high if set

EX3: External interrupt 3 enable if set

IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced

IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software

PX2: External interrupt 2 priority high if set

EX2: External interrupt 2 enable if set

IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced

IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

Eight-source interrupt information

INTERRUPT SOURCE	VECTOR ADDRESS	POLLING SEQUENCE WITHIN PRIORITY LEVEL	ENABLE REQUIRED SETTINGS	INTERRUPT TYPE EDGE/LEVEL
External Interrupt 0	03H	0 (highest)	IE.0	TCON.0
Timer/Counter 0	0BH	1	IE.1	-
External Interrupt 1	13H	2	IE.2	TCON.2
Timer/Counter 1	1BH	3	IE.3	-
Serial Port	23H	4	IE.4	-
Timer/Counter 2	2BH	5	IE.5	-
External Interrupt 2	33H	6	XICON.2	XICON.0
External Interrupt 3	3BH	7 (lowest)	XICON.6	XICON.3

P4CONB (C3H)

BIT	NAME	FUNCTION
7, 6	P43FUN1 P43FUN0	00: Mode 0. P4.3 is a general purpose I/O port which is the same as Port1. 01: Mode 1. P4.3 is a Read Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1 and P43CMP0. 10: Mode 2. P4.3 is a Write Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1 and P43CMP0. 11: Mode 3. P4.3 is a Read/Write Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1, and P43CMP0.
5, 4	P43CMP1 P43CMP0	Chip-select signals address comparison: 00: Compare the full address (16 bits length) with the base address register P43AH, P43AL. 01: Compare the 15 high bits (A15 – A1) of address bus with the base address register P43AH, P43AL. 10: Compare the 14 high bits (A15 – A2) of address bus with the base address register P43AH, P43AL. 11: Compare the 8 high bits (A15 – A8) of address bus with the base address register P43AH, P43AL.
3, 2	P42FUN1 P42FUN0	The P4.2 function control bits which are the similar definition as P43FUN1, P43FUN0.
1, 0	P42CMP1 P42CMP0	The P4.2 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.

P4CONA (C2H)

BIT	NAME	FUNCTION
7, 6	P41FUN1 P41FUN0	The P4.1 function control bits which are the similar definition as P43FUN1, P43FUN0.
5, 4	P41CMP1 P41CMP0	The P4.1 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.
3, 2	P40FUN1 P40FUN0	The P4.0 function control bits which are the similar definition as P43FUN1, P43FUN0.
1, 0	P40CMP1 P40CMP0	The P4.0 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.

P2ECON (AEH)

BIT	NAME	FUNCTION
7	P43CSINV	The active polarity of P4.3 when pin P4.3 is defined as read and/or write strobe signal. = 1: P4.3 is active high when pin P4.3 is defined as read and/or write strobe signal. = 0: P4.3 is active low when pin P4.3 is defined as read and/or write strobe signal.
6	P42CSINV	The similarity definition as P43SINV.
5	P41CSINV	The similarity definition as P43SINV.
5	P41CSINV	The similarity definition as P43SINV.
4	P40CSINV	The similarity definition as P43SINV.
3	-	Reserve
2	-	Reserve
1	-	0
0	-	0

5.11 Port 4 Base Address Registers

P40AH, P40AL:

The Base address register for comparator of P4.0. P40AH contains the high-order byte of address, P40AL contains the low-order byte of address.

P41AH, P41AL:

The Base address register for comparator of P4.1. P41AH contains the high-order byte of address, P41AL contains the low-order byte of address.

P42AH, P42AL:

The Base address register for comparator of P4.2. P42AH contains the high-order byte of address, P42AL contains the low-order byte of address.

P43AH, P43AL:

The Base address register for comparator of P4.3. P43AH contains the high-order byte of address, P43AL contains the low-order byte of address.

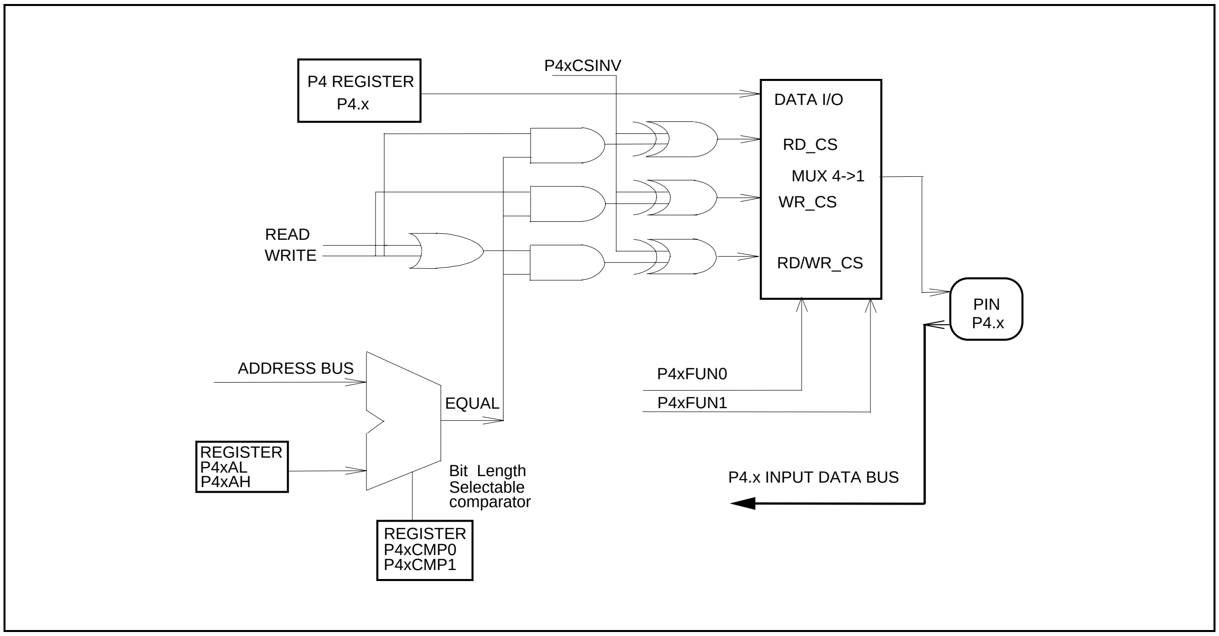
P4 (D8H)

BIT	NAME	FUNCTION
7	-	Reserve
6	-	Reserve
5	-	Reserve
4	-	Reserve
3	P43	Port 4 Data bit which outputs to pin P4.3 at mode 0.
2	P42	Port 4 Data bit which outputs to pin P4.2 at mode 0.
1	P41	Port 4 Data bit which outputs to pin P4.1at mode 0.
0	P40	Port 4 Data bit which outputs to pin P4.0 at mode 0.

Here is an example to program the P4.0 as a write strobe signal at the I/O port address 1234H – 1237H and positive polarity, and P4.1 – P4.3 are used as general I/O ports.

```
MOV  P40AH, #12H
MOV  P40AL, #34H          ; Base I/O address 1234H for P4.0
MOV  P4CONA, #00001010B   ; P4.0 a write strobe signal and address line A0 and A1 are masked.
MOV  P4CONB, #00H         ; P4.1 – P4.3 as general I/O port which are the same as PORT1
MOV  P2ECON, #10H         ; Write the P40SINV = 1 to inverse the P4.0 write strobe polarity
                          ; default is negative.
```

Then any instruction MOVX @DPTR, A (with DPTR = 1234H – 1237H) will generate the positive polarity write strobe signal at pin P4.0. And the instruction MOV P4, #XX will output the bit3 to bit1 of data #XX to pin P4.3 – P4.1.



5.12 In-System Programming (ISP) Mode

The W78E516B equips one 64K byte of main Flash EPROM bank for application program (called APROM) and one 4K byte of auxiliary Flash EPROM bank for loader program (called LDROM). In the normal operation, the microcontroller executes the code in the APROM. If the content of APROM needs to be modified, the W78E516B allows user to activate the In-System Programming (ISP) mode by setting the CHPCON register. **The CHPCON is read-only by default, software must write two specific values 87H, then 59H sequentially to the CHPENR register to enable the CHPCON write attribute. Writing CHPENR register with the values except 87H and 59H will close CHPCON register write attribute.** The W78E516B achieves all in-system programming operations including enter/exit ISP Mode, program, erase, read ... etc, during device in the idle mode. Setting the bit CHPCON.0 the device will enter in-system programming mode after a wake-up from idle mode. Because device needs proper time to complete the ISP operations before awaken from idle mode, software may use timer interrupt to control the duration for device wake-up from idle mode. To perform ISP operation for revising contents of APROM, software located at APROM setting the CHPCON register then enter idle mode, after awaken from idle mode the device executes the corresponding interrupt service routine in LDROM. Because the device will clear the program counter while switching from APROM to LDROM, the first execution of RETI instruction in interrupt service routine will jump to 00H at LDROM area. The device offers a software reset for switching back to APROM while the content of APROM has been updated completely. **Setting CHPCON register bit 0, 1 and 7 to logic-1 will result a software reset to reset the CPU**. The software reset serves as a external reset. This in-system programming feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-system programming feature make it possible to easily update the system firmware without opening the chassis.

SFRAH, SFRAL: The objective address of on-chip Flash EPROM in the in-system programming mode. SFRFAH contains the high-order byte of address, SFRFAL contains the low-order byte of address.

SFRFD: The programming data for on-chip Flash EPROM in programming mode.

SFRCN: The control byte of on-chip Flash EPROM programming mode.

SFRCN (C7)

BIT	NAME	FUNCTION
7	-	Reserve.
6	WFWIN	On-chip Flash EPROM bank select for in-system programming. = 0: 64K bytes Flash EPROM bank is selected as destination for re-programming. = 1: 4K bytes Flash EPROM bank is selected as destination for re-programming.
5	OEN	Flash EPROM output enable.
4	CEN	Flash EPROM chip enable.
3, 2, 1, 0	CTRL[3:0]	The flash control signals

MODE	WFWIN	CTRL<3:0>	OEN	CEN	SFRAH, SFRAL	SFRFD
Erase 64KB APROM	0	0010	1	0	X	X
Program 64KB APROM	0	0001	1	0	Address in	Data in
Read 64KB APROM	0	0000	0	0	Address in	Data out
Erase 4KB LDROM	1	0010	1	0	X	X
Program 4KB LDROM	1	0001	1	0	Address in	Data in
Read 4KB LDROM	1	0000	0	0	Address in	Data out

5.13 In-System Programming Control Register (CHPCON)

CHPCON (BFH)

BIT	NAME	FUNCTION
7	SWRESET (F04KMODE)	When this bit is set to 1, and both FBOOTSL and FPROGEN are set to 1. It will enforce microcontroller reset to initial condition just like power on reset. This action will re-boot the microcontroller and start to normal operation. To read this bit in logic-1 can determine that the F04KBOOT mode is running.
6	-	Reserve.
5	-	Reserve.
4	ENAUXRAM	1: Enable on-chip AUX-RAM. 0: Disable the on-chip AUX-RAM
3	0	Must set to 0.
2	0	Must set to 0.
1	FBOOTSL	The Program Location Select. 0: The Loader Program locates at the 64 KB APROM. 4KB LDROM is destination for re-programming. 1: The Loader Program locates at the 4 KB memory bank. 64KB APROM is destination for re-programming.
0	FPROGEN	FLASH EPROM Programming Enable. = 1: enable. The microcontroller enter the in-system programming mode after entering the idle mode and wake-up from interrupt. During in-system programming mode, the operation of erase, program and read are achieve when device enters idle mode. = 0: disable. The on-chip flash memory is read-only. In-system programmability is disabled.

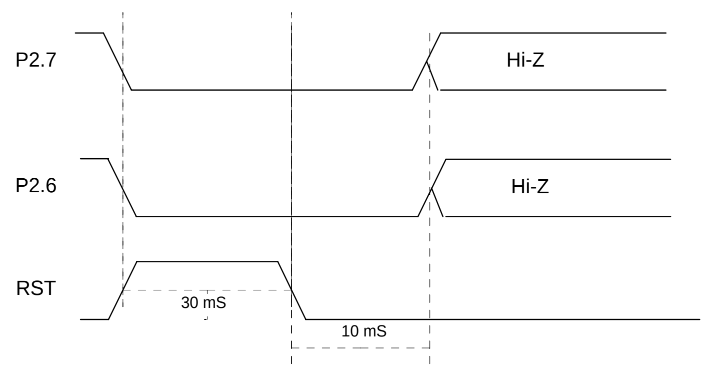
F04KBOOT Mode (Boot from LDROM)

By default, the W78E516B boots from APROM program after a power on reset. On some occasions, user can force the W78E516B to boot from the LDROM program via following settings. The possible situation that you need to enter F04KBOOT mode when the APROM program can not run properly and device can not jump back to LDROM to execute in-system programming function. Then you can use this F04KBOOT mode to force the W78E516B jumps to LDROM and executes in-system programming procedure. When you design your system, you may reserve the pins P2.6, P2.7 to switches or jumpers. For example in a CD-ROM system, you can connect the P2.6 and P2.7 to PLAY and EJECT buttons on the panel. When the APROM program fails to execute the normal application program. User can press both two buttons at the same time and then turn on the power of the personal computer to force the W78E516B to enter the F04KBOOT mode. After power on of personal computer, you can release both buttons and finish the in-system programming procedure to update the APROM code. In application system design, user must take care of the P2, P3, ALE, $\overline{\text{EA}}$ and $\overline{\text{PSEN}}$ pin value at reset to prevent from accidentally activating the programming mode or F04KBOOT mode.

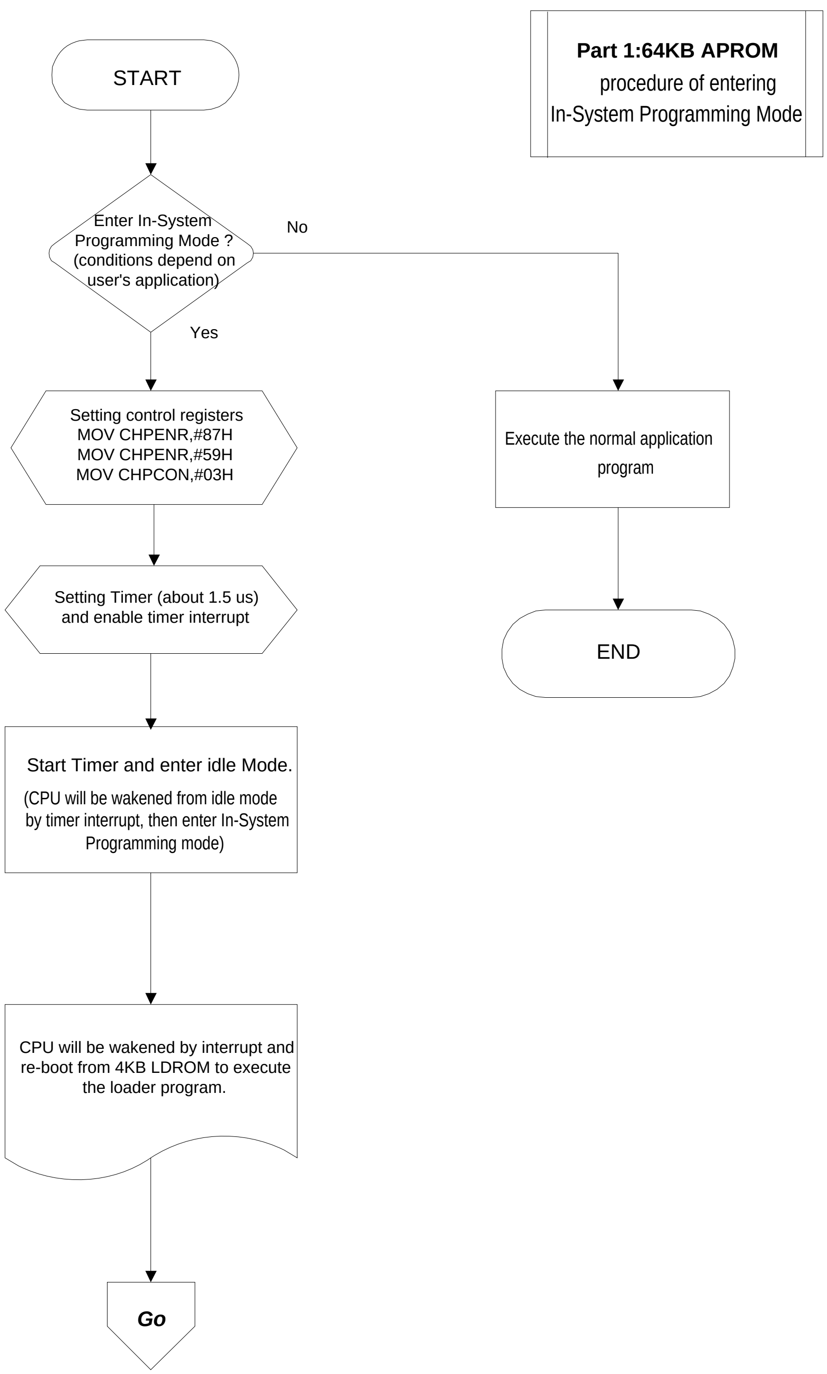
F04KBOOT MODE

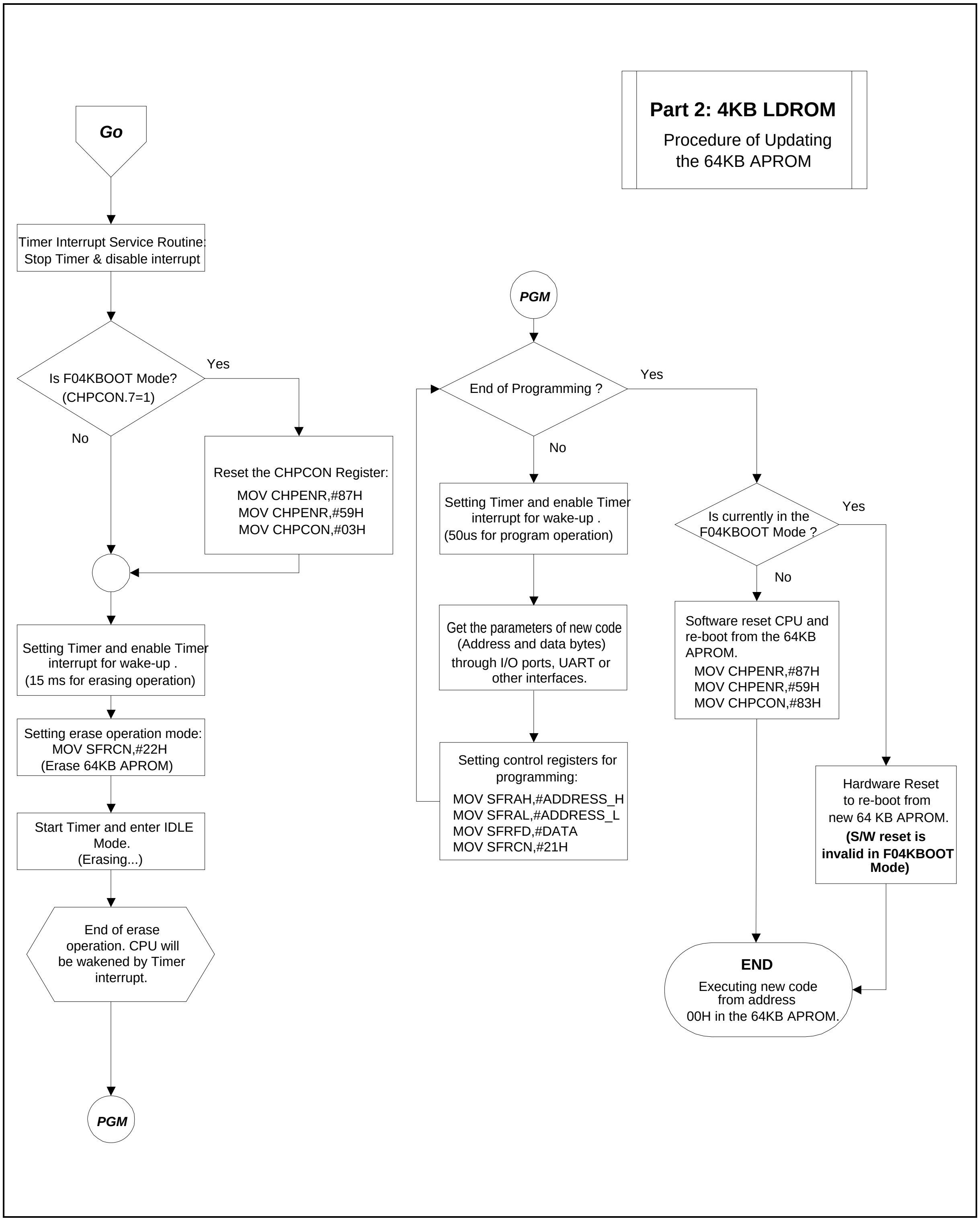
P4.3	P2.7	P2.6	MODE
X	L	L	FO4KBOOT
L	X	X	FO4KBOOT

The Reset Timing For Entering F04KBOOT Mode



The Algorithm of In-System Programming

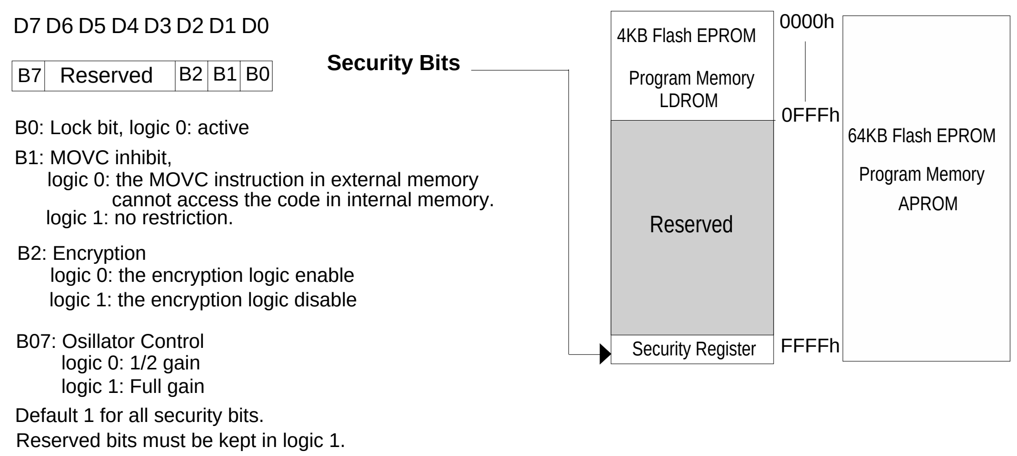



Part 2: 4KB LDROM
Procedure of Updating the 64KB APROM
Go
Timer Interrupt Service Routine: Stop Timer & disable interrupt
Is F04KBOOT Mode? (CHPCON.7=1)
Yes
No
Reset the CHPCON Register:
MOV CHPENR,#87H
MOV CHPENR,#59H
MOV CHPCON,#03H
Setting Timer and enable Timer interrupt for wake-up . (15 ms for erasing operation)
Setting erase operation mode: MOV SFRCN,#22H (Erase 64KB APROM)
Start Timer and enter IDLE Mode. (Erasing...)
End of erase operation. CPU will be wakened by Timer interrupt.
PGM
PGM
End of Programming ?
Yes
No
Setting Timer and enable Timer interrupt for wake-up . (50us for program operation)
Get the parameters of new code (Address and data bytes) through I/O ports, UART or other interfaces.
Setting control registers for programming:
MOV SFRAH,#ADDRESS_H
MOV SFRAL,#ADDRESS_L
MOV SFRFD,#DATA
MOV SFRCN,#21H
Is currently in the F04KBOOT Mode ?
Yes
No
Software reset CPU and re-boot from the 64KB APROM.
MOV CHPENR,#87H
MOV CHPENR,#59H
MOV CHPCON,#83H
Hardware Reset to re-boot from new 64 KB APROM.
(S/W reset is invalid in F04KBOOT Mode)
END
Executing new code from address 00H in the 64KB APROM.

6. SECURITY

During the on-chip Flash EPROM programming mode, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of Flash EPROM and those operations on it are described below.

The W78E516B has a Special Setting Register, the Security Register, which can not be accessed in programming mode. Those bits of the Security Register can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The Security Register is located at the 0FFFFH of the LDROM space.



Special Setting Register

6.1 Lock Bit

This bit is used to protect the customer's program code in the W78E516B. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and Special Setting Registers can not be accessed again.

6.2 MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

6.3 Encryption

This bit is used to enable/disable the encryption logic for code protection. Once encryption feature is enabled, the data presented on port 0 will be encoded via encryption logic. Only whole chip erase will reset this bit.

6.4 Oscillator Control

W78E516B/E516 allow user to diminish the gain of on-chip oscillator amplifier by using programmer to set the bit B7 of security register. Once B7 is set to 0, a half of gain will be decreased. Care must be taken if user attempts to diminish the gain of oscillator amplifier, reducing a half of gain may improperly affect the external crystal operation at high frequency above 24 MHz. The value of R and C1, C2 may need some adjustment while running at lower gain.

7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	$V_{DD} - V_{SS}$	-0.3	+6.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{ST}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2 D.C. Characteristics

($V_{DD} - V_{SS}$ = 5V ±10%, T_A = 25°C, Fosc = 20 MHz, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Operating Voltage	V_{DD}	4.5	5.5	V	RST = 1, P0 = V_{DD}
Operating Current	I_{DD}	-	20	mA	No load V_{DD} = 5.5V
Idle Current	I_{IDLE}	-	6	mA	Idle mode V_{DD} = 5.5V
Power Down Current	I_{PWDN}	-	50	μA	Power-down mode V_{DD} = 5.5V
Input Current P1, P2, P3, P4	I_{IN1}	-50	+10	μA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}
Input Current RST	I_{IN2}	-10	+300	μA	V_{DD} = 5.5V 0< V_{IN} <V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK}	-10	+10	μA	V_{DD} = 5.5V 0V< V_{IN} < V_{DD}
Logic 1 to 0 Transition Current P1, P2, P3, P4	I_{TL}[*4]	-500	-	μA	V_{DD} = 5.5V V_{IN} = 2.0V
Input Low Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IL1}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage RST	VIL2	0	0.8	V	VDD = 4.5V
Input Low Voltage XTAL1[*4]	VIL3	0	0.8	V	VDD = 4.5V

D.C. Characteristics, continued

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Input High Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IH1}	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage RST	V_{IH2}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage XTAL1[*4]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Output Low Voltage P1, P2, P3, P4	V_{OL1}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +2 mA
Output Low Voltage P0, ALE, $\overline{PSEN}$ [*3]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +4 mA
Sink Current P1, P3, P4	Isk1	4	12	mA	V_{DD} = 4.5V V_{IN} = 0.45V
Sink Current P0, P2, ALE, $\overline{PSEN}$	Isk2	10	20	mA	V_{DD} = 4.5V V_{IN} = 0.45V
Output High Voltage P1, P2, P3, P4	V_{OH1}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -100 μA
Output High Voltage P0, ALE, $\overline{PSEN}$ [*3]	V_{OH2}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -400 μA
Source Current P1, P2, P3, P4	Isr1	-120	-250	μA	V_{DD} = 4.5V V_{IN} = 2.4V
Source Current P0, P2, ALE, $\overline{PSEN}$	Isr2	-8	-20	mA	V_{DD} = 4.5V V_{IN} = 2.4V

Notes:

*1. RST pin is a Schmitt trigger input.

*3. P0, ALE and $\overline{PSEN}$ are tested in the external access mode.

*4. XTAL1 is a CMOS input.

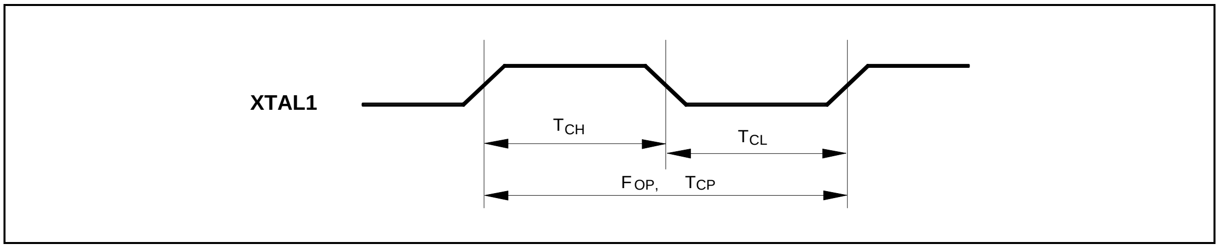
*5. Pins of P1, P2, P3, P4 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} approximates to 2V.

Publication Release Date: December 4, 2006
Revision A11

7.3 A.C. Characteristics

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.6 micron CMOS process when using 2 and 4 mA output buffers.

7.3.1 Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	Fop	0	-	40	MHz	1
Clock Period	TCP	25	-	-	nS	2
Clock High	Tch	10	-	-	nS	3
Clock Low	Tcl	10	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The TCP specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

7.3.2 Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 TCP-Δ	-	-	nS	4
Address Hold from ALE Low	TAAH	1 TCP-Δ	-	-	nS	1, 4
ALE Low to $\overline{\text{PSEN}}$ Low	TAPL	1 TCP-Δ	-	-	nS	4
$\overline{\text{PSEN}}$ Low to Data Valid	TPDA	-	-	2 TCP	nS	2
Data Hold after $\overline{\text{PSEN}}$ High	TPDH	0	-	1 TCP	nS	3
Data Float after $\overline{\text{PSEN}}$ High	TPDZ	0	-	1 TCP	nS	
ALE Pulse Width	TALW	2 TCP-Δ	2 TCP	-	nS	4
$\overline{\text{PSEN}}$ Pulse Width	TPSW	3 TCP-Δ	3 TCP	-	nS	4

Notes:

1. P0.0 – P0.7, P2.0 – P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TCP.
3. Data have been latched internally prior to $\overline{\text{PSEN}}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

7.3.3 Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{RD}$ Low	T_{DAR}	$3\ T_{CP}-\Delta$	-	$3\ T_{CP}+\Delta$	nS	1, 2
$\overline{RD}$ Low to Data Valid	T_{DDA}	-	-	$4\ T_{CP}$	nS	1
Data Hold from $\overline{RD}$ High	T_{DDH}	0	-	$2\ T_{CP}$	nS	
Data Float from $\overline{RD}$ High	T_{DDZ}	0	-	$2\ T_{CP}$	nS	
$\overline{RD}$ Pulse Width	T_{DRD}	$6\ T_{CP}-\Delta$	$6\ T_{CP}$	-	nS	2

Notes:

1. Data memory access time is 8 T_{CP}.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

7.3.4 Data Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	T_{DAW}	$3\ T_{CP}-\Delta$	-	$3\ T_{CP}+\Delta$	nS
Data Valid to $\overline{WR}$ Low	T_{DAD}	$1\ T_{CP}-\Delta$	-	-	nS
Data Hold from $\overline{WR}$ High	T_{DWD}	$1\ T_{CP}-\Delta$	-	-	nS
$\overline{WR}$ Pulse Width	T_{DWR}	$6\ T_{CP}-\Delta$	$6\ T_{CP}$	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

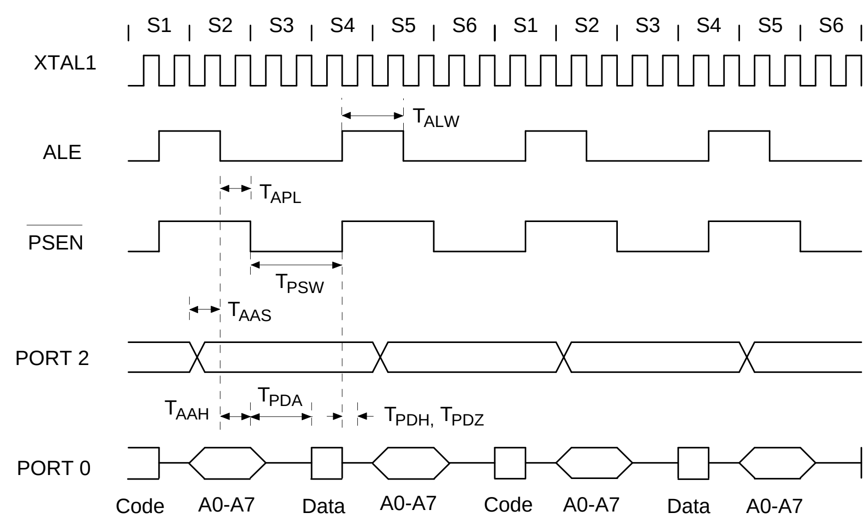
7.3.5 Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	T_{PDS}	1 TCP	-	-	nS
Port Input Hold from ALE Low	T_{PDH}	0	-	-	nS
Port Output to ALE	T_{PDA}	1 TCP	-	-	nS

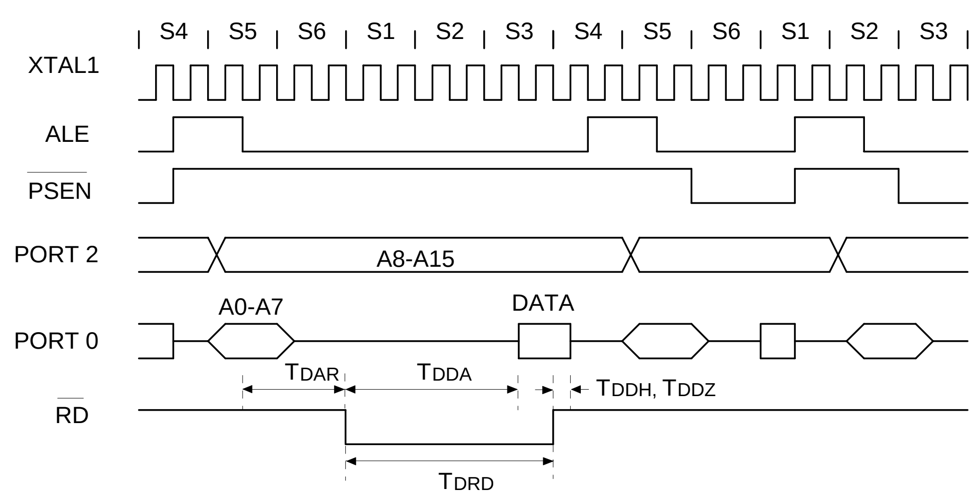
Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

8. TIMING WAVEFORMS

8.1 Program Fetch Cycle

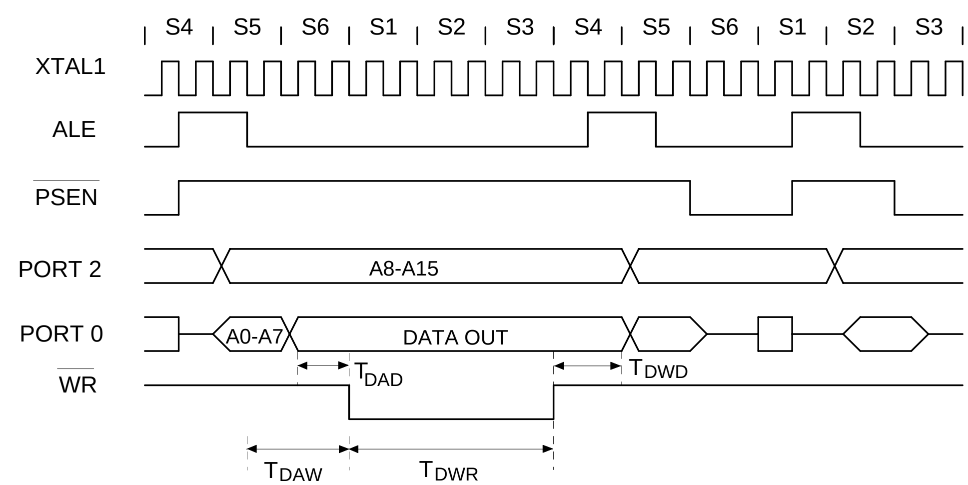


8.2 Data Read Cycle

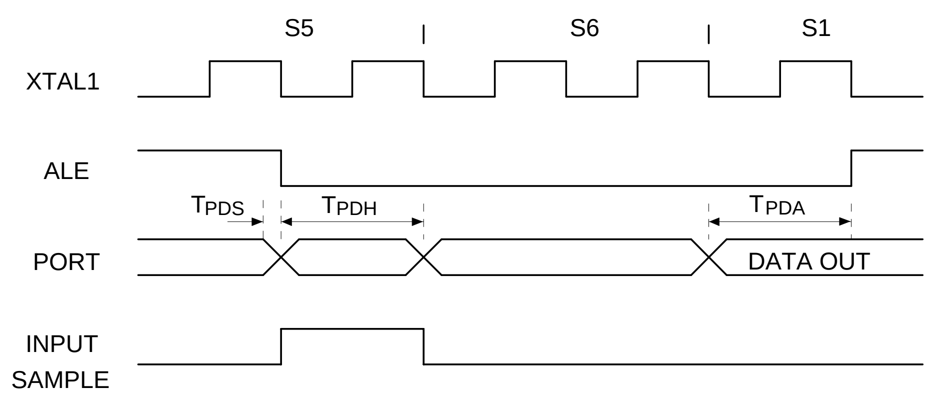


Timing Waveforms, continued

8.3 Data Write Cycle



8.4 Port Access Cycle



9. TYPICAL APPLICATION CIRCUITS

9.1 External Program Memory and Crystal

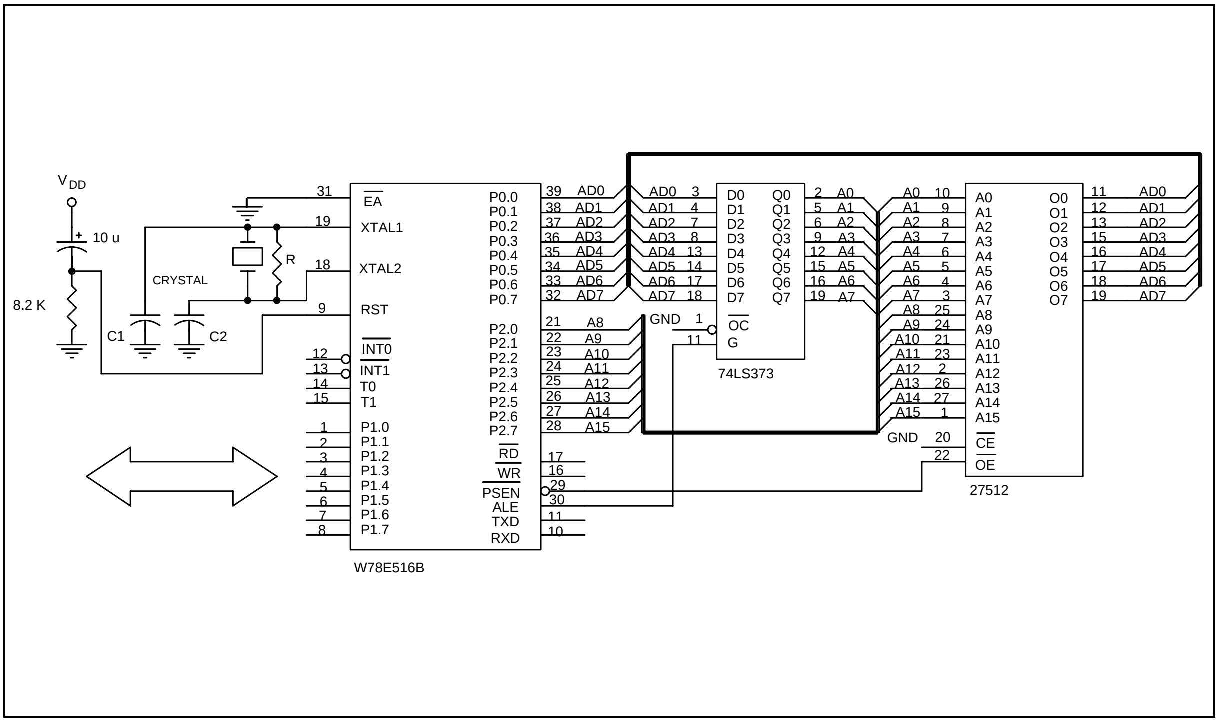


Figure A

CRYSTAL	C1	C2	R
6 MHz	47P	47P	-
16 MHz	30P	30P	-
24 MHz	15P	10P	-
32 MHz	10P	10P	6.8K
40 MHz	5P	5P	4.7K

Above table shows the reference values for crystal applications.

Notes:

1. C1, C2, R components refer to Figure A
2. Crystal layout must get close to XTAL1 and XTAL2 pins on user's application board.

Typical Application Circuits, continued

9.2 Expanded External Data Memory and Oscillator

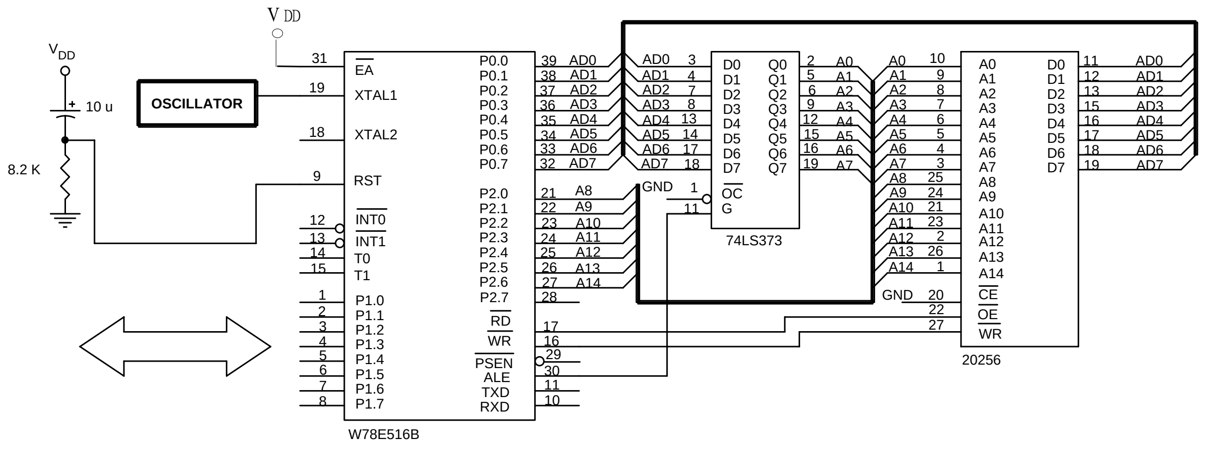
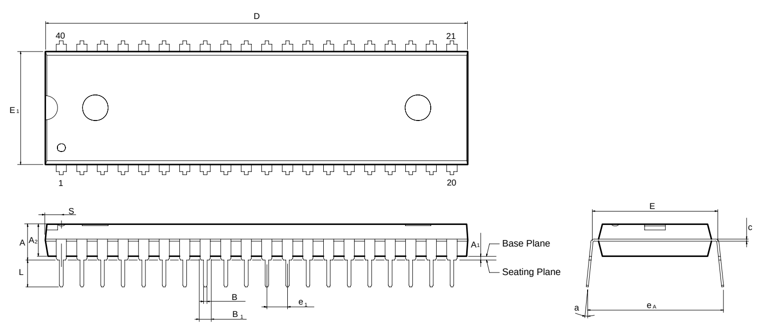


Figure B

10. PACKAGE DIMENSIONS

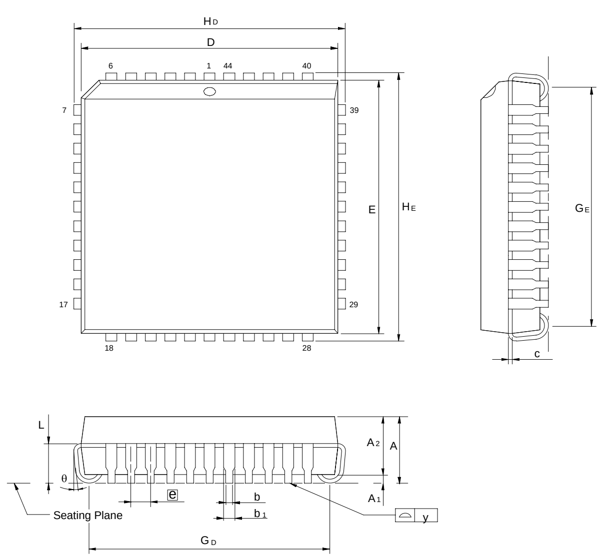
10.1 40-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

10.2 44-pin PLCC

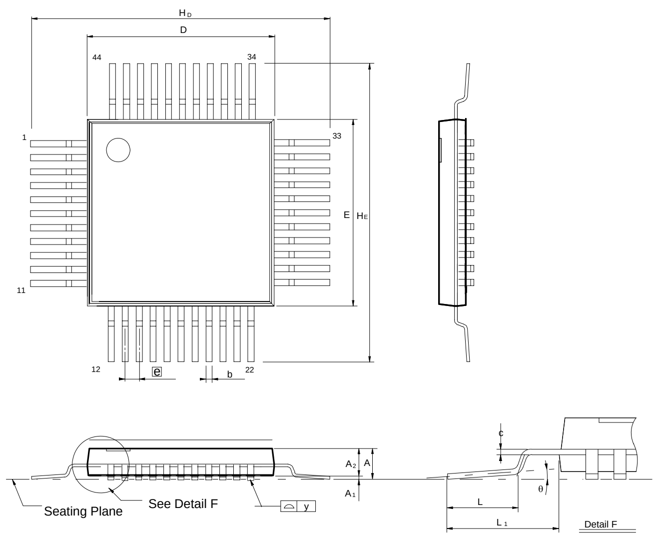


Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e		0.050 BSC			1.27 BSC	
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

Package Dimensions, continued.

10.3 44-pin PQFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

11. APPLICATION NOTE

11.1 In-system Programming Software Examples

This application note illustrates the in-system programmability of the Winbond W78E516B Flash EPROM microcontroller. In this example, microcontroller will boot from 64 KB APROM bank and waiting for a key to enter in-system programming mode for re-programming the contents of 64 KB APROM. While entering in-system programming mode, microcontroller executes the loader program in 4KB LDROM bank. The loader program erases the 64 KB APROM then reads the new code data from external SRAM buffer (or through other interfaces) to update the 64KB APROM.

EXAMPLE 1:

```
;*****************************************************************************************************
;* Example of 64K APROM program: Program will scan the P1.0. if P1.0 = 0, enters in-system
;* programming mode for updating the content of APROM code else executes the current ROM code.
;* XTAL = 40 MHz
;*****************************************************************************************************
        .chip 8052
        .RAMCHK OFF
        .symbols

        CHPCON    EQU    BFH
        CHPENR    EQU    F6H
        SFRAL     EQU    C4H
        SFRAH     EQU    C5H
        SFRFD     EQU    C6H
        SFRCN     EQU    C7H

        ORG    0H
        LJMP   100H             ; JUMP TO MAIN PROGRAM
   ;************************************************************************
   ;*  TIMER0 SERVICE VECTOR ORG = 000BH
   ;************************************************************************
        ORG    00BH
        CLR    TR0                     ; TR0 = 0, STOP TIMER0
        MOV    TL0, R6
        MOV    TH0, R7
        RETI
   ;************************************************************************
   ;*  64K APROM MAIN PROGRAM
   ;************************************************************************
       ORG 100H

MAIN_64K:
       MOV A, P1                        ; SCAN P1.0
       ANL A, #01H
       CJNE A, #01H, PROGRAM_64K   ; IF P1.0 = 0, ENTER IN-SYSTEM PROGRAMMING MODE
       JMP NORMAL_MODE

PROGRAM_64K:
        MOV CHPENR, #87H            ; CHPENR = 87H, CHPCON REGISTER WRTE ENABLE
        MOV CHPENR, #59H            ; CHPENR = 59H, CHPCON REGISTER WRITE ENABLE
        MOV CHPCON, #03H            ; CHPCON = 03H, ENTER IN-SYSTEM PROGRAMMING MODE
         MOV TCON, #00H             ; TR = 0 TIMER0 STOP
```

```
        MOV IP, #00H                ; IP = 00H
        MOV IE, #82H                ; TIMER0 INTERRUPT ENABLE FOR WAKE-UP FROM IDLE MODE
        MOV R6, #F0H                ; TL0 = F0H
        MOV R7, #FFH                ; TH0 = FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV TMOD, #01H              ; TMOD = 01H, SET TIMER0 A 16-BIT TIMER
        MOV TCON, #10H              ; TCON = 10H, TR0 = 1,GO
        MOV PCON, #01H              ; ENTER IDLE MODE FOR LAUNCHING THE IN-SYSTEM
                                    ; PROGRAMMABILITY
;*********************************************************************************
;* Normal mode 64KB APROM program: depending user's application
;*********************************************************************************
NORMAL_MODE:
        .                           ; User's application program
        .
        .
        .
```

EXAMPLE 2:

```
;*********************************************************************************************************************** ;*
Example of 4KB LDROM program: This lorder program will erase the 64KB APROM first, then reads the new ;*
code from external SRAM and program them into 64KB APROM bank. XTAL = 40 MHz
;***********************************************************************************************************************
    .chip 8052
    .RAMCHK OFF
    .symbols

    CHPCON    EQU    BFH
    CHPENR    EQU    F6H
    SFRAL     EQU    C4H
    SFRAH     EQU    C5H
    SFRFD     EQU    C6H
    SFRCN     EQU    C7H

        ORG    000H
        LJMP   100H                 ; JUMP TO MAIN PROGRAM
  ;************************************************************************
  ;* 1. TIMER0 SERVICE VECTOR ORG = 0BH
  ;************************************************************************
        ORG 000BH
        CLR   TR0                   ; TR0 = 0, STOP TIMER0
        MOV TL0, R6
        MOV TH0, R7
        RETI
;************************************************************************
  ;*  4KB LDROM MAIN PROGRAM
  ;************************************************************************
       ORG 100H
```

```
MAIN_4K:
        MOV SP, #C0H            ; BE INITIAL SP REGISTER
        MOV CHPENR, #87H        ; CHPENR = 87H, CHPCON WRITE ENABLE.
        MOV CHPENR, #59H        ; CHPENR = 59H, CHPCON WRITE ENABLE.
        MOV A, CHPCON
        ANL A, #80H
        CJNE A, #80H, UPDATE_64K   ; CHECK  F04KBOOT MODE ?

        MOV CHPCON, #03H        ; CHPCON = 03H, ENABLE IN-SYSTEM PROGRAMMING.
        MOV CHPENR, #00H        ; DISABLE CHPCON WRITE ATTRIBUTE

        MOV TCON, #00H          ; TCON = 00H, TR = 0 TIMER0 STOP
        MOV TMOD, #01H          ; TMOD = 01H, SET TIMER0 A 16BIT TIMER
        MOV IP, #00H            ; IP = 00H
        MOV IE, #82H            ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV R6, #F0H
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV TCON, #10H          ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H          ; ENTER IDLE MODE

UPDATE_64K:
        MOV CHPENR, #00H        ; DISABLE CHPCON WRITE-ATTRIBUTE
        MOV TCON, #00H          ; TCON = 00H, TR = 0 TIM0 STOP
        MOV IP, #00H            ; IP = 00H
        MOV IE, #82H            ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV TMOD, #01H          ; TMOD = 01H, MODE1
        MOV R6, #3CH            ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15 mS. DEPENDING
                                ; ON USER'S SYSTEM CLOCK RATE.
        MOV R7, #B0H
        MOV TL0, R6
        MOV TH0, R7

ERASE_P_4K:
        MOV SFRCN, #22H         ; SFRCN(C7H) = 22H  ERASE 64K
        MOV TCON, #10H          ; TCON = 10H, TR0 = 1,GO
        MOV PCON, #01H          ; ENTER IDLE MODE (FOR ERASE OPERATION)

;*********************************************************************
;* BLANK CHECK
;*********************************************************************
        MOV SFRCN, #0H          ; READ 64KB APROM MODE
        MOV SFRAH, #0H          ; START ADDRESS = 0H
        MOV SFRAL, #0H
        MOV R6, #FBH            ; SET TIMER FOR READ OPERATION, ABOUT 1.5 µS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7

BLANK_CHECK_LOOP:
        SETB TR0                ; ENABLE TIMER 0
        MOV PCON, #01H          ; ENTER IDLE MODE
        MOV A, SFRFD            ; READ ONE BYTE
        CJNE A, #FFH, BLANK_CHECK_ERROR
```

```
        INC SFRAL                   ; NEXT ADDRESS
        MOV A, SFRAL
        JNZ BLANK_CHECK_LOOP
        INC SFRAH
        MOV A, SFRAH
        CJNE A, #0H, BLANK_CHECK_LOOP   ; END ADDRESS = FFFFH
        JMP PROGRAM_64KROM

BLANK_CHECK_ERROR:
        MOV P1, #F0H
        MOV P3, #F0H
        JMP $

;*********************************************************************************
;* RE-PROGRAMMING 64KB APROM BANK
;*********************************************************************************
PROGRAM_64KROM:
        MOV DPTR, #0H               ; THE ADDRESS OF NEW ROM CODE
        MOV R2, #00H                ; TARGET LOW BYTE ADDRESS
        MOV R1, #00H                ; TARGET HIGH BYTE ADDRESS
        MOV DPTR, #0H               ; EXTERNAL SRAM BUFFER ADDRESS
        MOV SFRAH, R1               ; SFRAH, TARGET HIGH ADDRESS
        MOV SFRCN, #21H             ; SFRCN (C7H) = 21 (PROGRAM 64K)
        MOV R6, #5AH                ; SET TIMER FOR PROGRAMMING, ABOUT 50 µS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7

PROG_D_64K:
        MOV SFRAL, R2               ; SFRAL (C4H) = LOW BYTE ADDRESS
        MOVX A, @DPTR               ; READ DATA FROM EXTERNAL SRAM BUFFER
        MOV SFRFD, A                ; SFRFD (C6H) = DATA IN
        MOV TCON, #10H              ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H              ; ENTER IDLE MODE (PRORGAMMING)
        INC DPTR
        INC R2
        CJNE R2, #0H, PROG_D_64K
        INC  R1
        MOV SFRAH, R1
        CJNE R1, #0H, PROG_D_64K

;*******************************************************************************
; * VERIFY 64KB APROM BANK
;*******************************************************************************
        MOV R4, #03H                ; ERROR COUNTER
        MOV R6, #FBH                ; SET TIMER FOR READ VERIFY, ABOUT 1.5 µS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV DPTR, #0H               ; The start address of sample code
        MOV R2, #0H                 ; Target low byte address
        MOV R1, #0H                 ; Target high byte address
        MOV SFRAH, R1               ; SFRAH, Target high address
        MOV SFRCN, #00H             ; SFRCN = 00 (Read ROM CODE)
```

```
READ_VERIFY_64K:
        MOV SFRAL, R2           ; SFRAL (C4H) = LOW ADDRESS
        MOV TCON, #10H          ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H
        INC R2
        MOVX A, @DPTR
        INC DPTR
        CJNE A, SFRFD, ERROR_64K
        CJNE R2, #0H, READ_VERIFY_64K
        INC R1
        MOV SFRAH, R1
        CJNE R1, #0H, READ_VERIFY_64K

;*******************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*******************************************************************************
        MOV CHPENR, #87H        ; CHPENR = 87H
        MOV CHPENR, #59H        ; CHPENR = 59H
        MOV CHPCON, #83H        ; CHPCON = 83H, SOFTWARE RESET.

ERROR_64K:
        DJNZ R4, UPDATE_64K     ; IF ERROR OCCURS, REPEAT 3 TIMES.
        .                       ; IN-SYSTEM PROGRAMMING FAIL, USER'S PROCESS TO DEAL WITH IT.
        .
        .
        .
```

12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A5	June, 2002	-	Formerly issued
A6	June, 2004	3	Revise part number in the item of packages
A7	Aug, 2004	26	Revise title of 10.1
A8	Jan, 2005	3	Add Lead Free package
A9	April 20, 2005	35	Add Important Notice
A10	October 2, 2006		Remove block diagram
A11	December 4, 2006	3	Remove all Leaded package parts